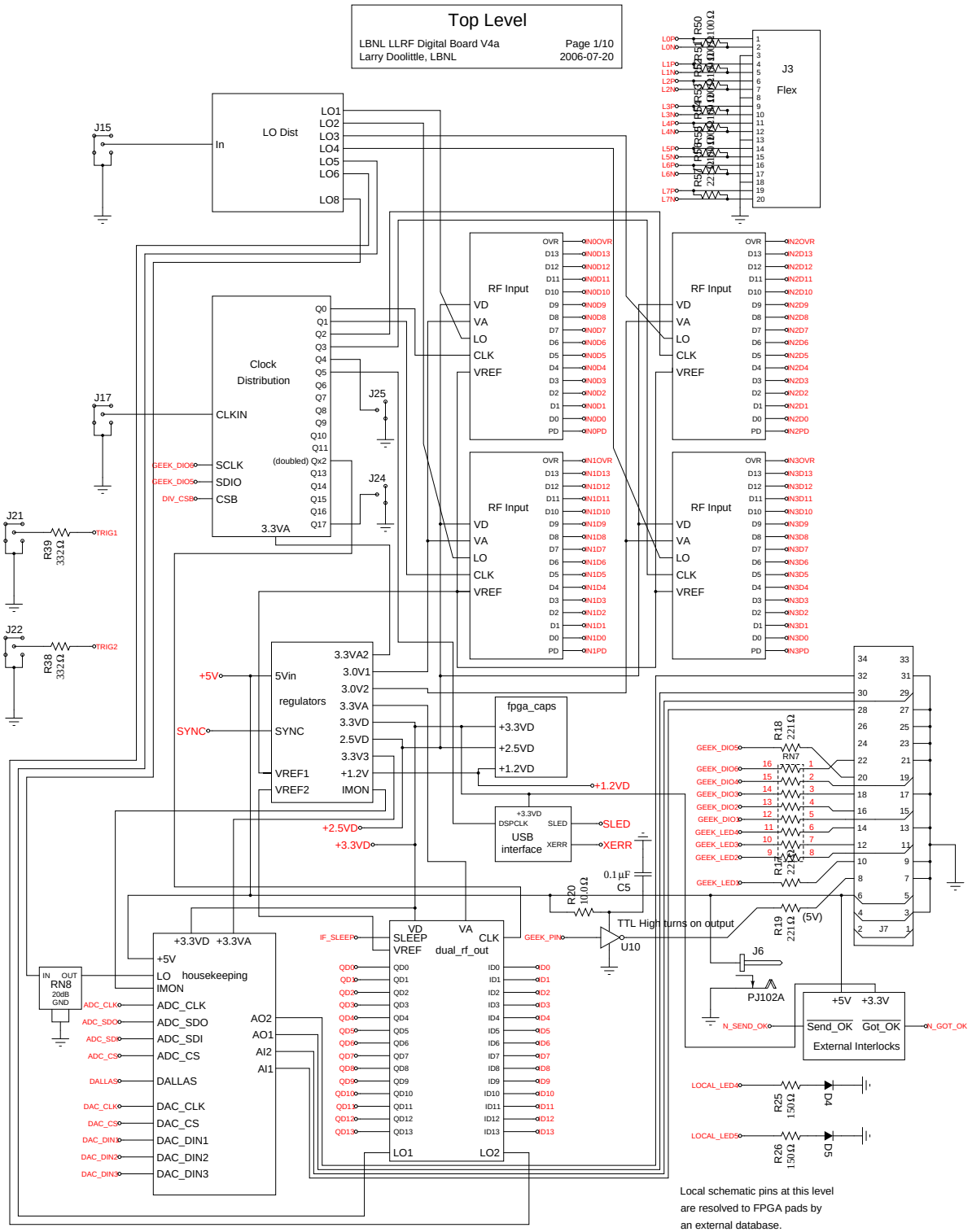
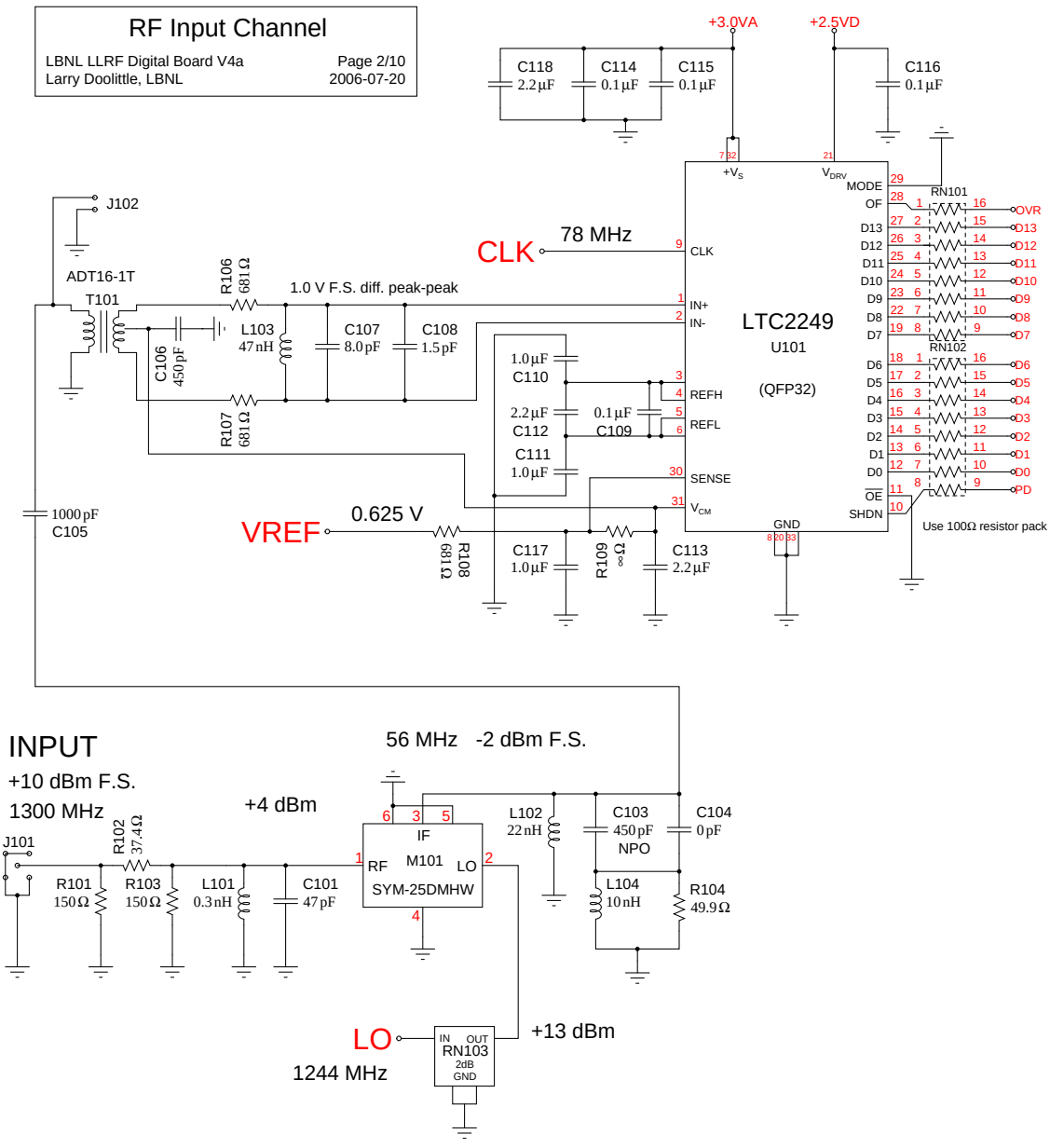

Top Level
LBNL LLRF Digital Board V4a
Larry Doolittle, LBNL
Page 1/10
2006-07-20
J3
Flex
LO Dist
In
LO1
LO2
LO3
LO4
LO5
LO6
LO8
J15
J17
J21
J22
J24
J25
Clock
Distribution
CLKIN
SCLK
SDIO
CSB
3.3VA
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
(doubled) Qx2
Q13
Q14
Q15
Q16
Q17
GEEK_DIO6
GEEK_DIO5
DIV_CSB
TRIG1
TRIG2
R39
332Ω
R38
332Ω
RF Input
VD
VA
LO
CLK
VREF
OVR
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
PD
N0OVR
N0D13
N0D12
N0D11
N0D10
N0D9
N0D8
N0D7
N0D6
N0D5
N0D4
N0D3
N0D2
N0D1
N0D0
N0PD
N2OVR
N2D13
N2D12
N2D11
N2D10
N2D9
N2D8
N2D7
N2D6
N2D5
N2D4
N2D3
N2D2
N2D1
N2D0
N2PD
N1OVR
N1D13
N1D12
N1D11
N1D10
N1D9
N1D8
N1D7
N1D6
N1D5
N1D4
N1D3
N1D2
N1D1
N1D0
N1PD
N3OVR
N3D13
N3D12
N3D11
N3D10
N3D9
N3D8
N3D7
N3D6
N3D5
N3D4
N3D3
N3D2
N3D1
N3D0
N3PD
+5V
SYNC
5Vin
regulators
SYNC
VREF1
VREF2
3.3VA2
3.0V1
3.0V2
3.3VA
3.3VD
2.5VD
3.3V3
+1.2V
IMON
fpga_caps
+3.3VD
+2.5VD
+1.2VD
+1.2VD
+2.5VD
+3.3VD
USB
interface
DSPCLK
SLED
XERR
SLED
XERR
0.1μF
C5
R20
10.0Ω
TTL High turns on output
U10
GEEK_PIN
IF_SLEEP
VD
VA
SLEEP
CLK
VREF
dual_rf_out
QD0
QD1
QD2
QD3
QD4
QD5
QD6
QD7
QD8
QD9
QD10
QD11
QD12
QD13
ID0
ID1
ID2
ID3
ID4
ID5
ID6
ID7
ID8
ID9
ID10
ID11
ID12
ID13
LO1
LO2
+3.3VD
+3.3VA
+5V
LO housekeeping
IMON
ADC_CLK
ADC_SDO
ADC_SDI
ADC_CS
DALLAS
DAC_CLK
DAC_CS
DAC_DIN1
DAC_DIN2
DAC_DIN3
AO2
AO1
AI2
AI1
RN8
20dB
IN
OUT
GND
R18
221Ω
RN7
R17
221Ω
R19
221Ω
(5V)
J7
J6
PJ102A
N_SEND_OK
+5V
+3.3V
Send_OK
Got_OK
N_GOT_OK
External Interlocks
LOCAL_LED4
LOCAL_LED5
R25
150Ω
R26
150Ω
D4
D5
Local schematic pins at this level
are resolved to FPGA pads by
an external database.


RF Input Channel
LBNL LLRF Digital Board V4a
Larry Doolittle, LBNL
Page 2/10
2006-07-20
+3.0VA
+2.5VD
C118 2.2µF
C114 0.1µF
C115 0.1µF
C116 0.1µF
+VS
VDRV
MODE
OF
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
OE
SHDN
RN101
RN102
OVR
PD
Use 100Ω resistor pack
J102
ADT16-1T
T101
R106 681Ω
R107 681Ω
1.0 V F.S. diff. peak-peak
CLK
78 MHz
CLK
IN+
IN-
LTC2249
U101
(QFP32)
REFH
REFL
SENSE
VCM
GND
L103 47nH
C106 450pF
C107 8.0pF
C108 1.5pF
1.0µF C110
2.2µF C112
0.1µF C109
C111 1.0µF
1000pF C105
VREF
0.625 V
R108 681Ω
C117 1.0µF
R109 ∞Ω
C113 2.2µF
INPUT
+10 dBm F.S.
1300 MHz
J101
R102 37.4Ω
R101 150Ω
R103 150Ω
L101 0.3nH
C101 47pF
+4 dBm
56 MHz -2 dBm F.S.
IF
RF
M101
LO
SYM-25DMHW
L102 22nH
C103 450pF NPO
C104 0pF
L104 10nH
R104 49.9Ω
LO
1244 MHz
IN OUT
RN103
2dB
GND
+13 dBm

USB Interface

LBNL LLRF Digital Board V4a — Page 3/10
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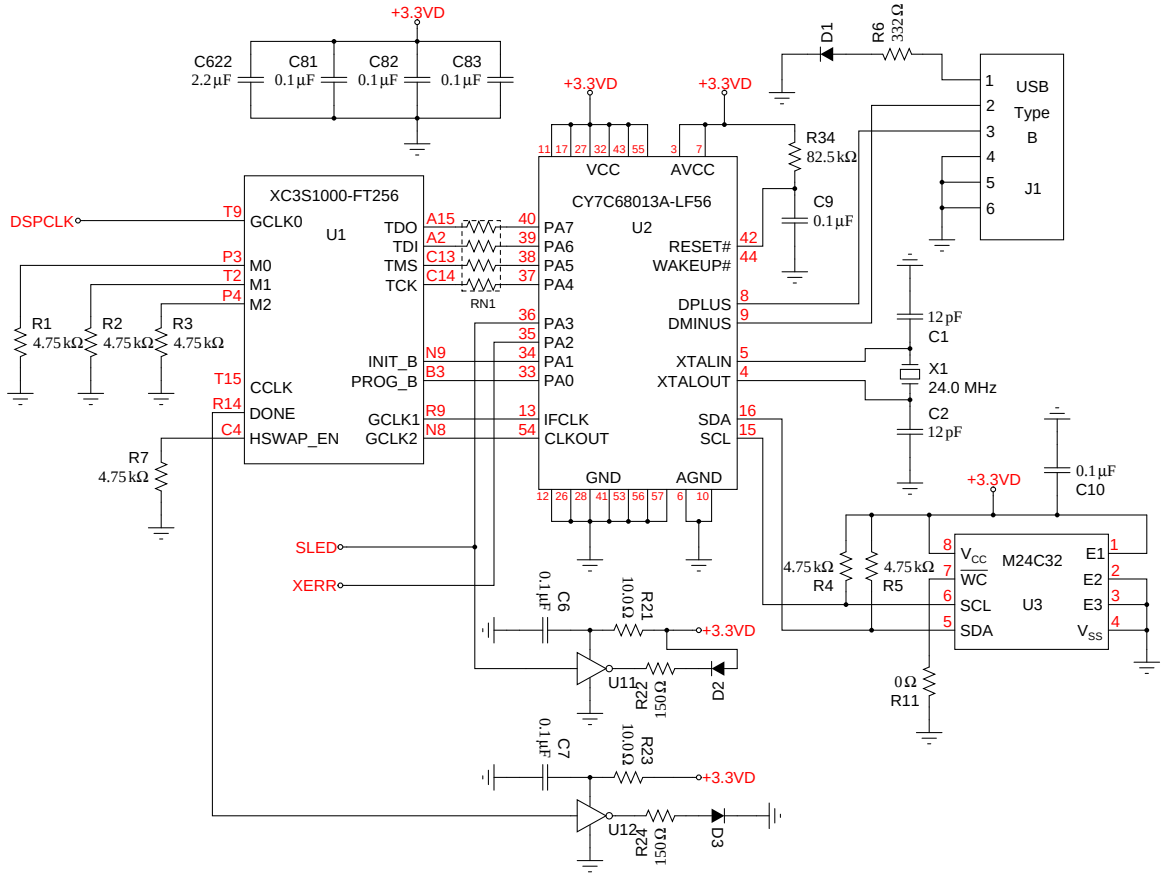

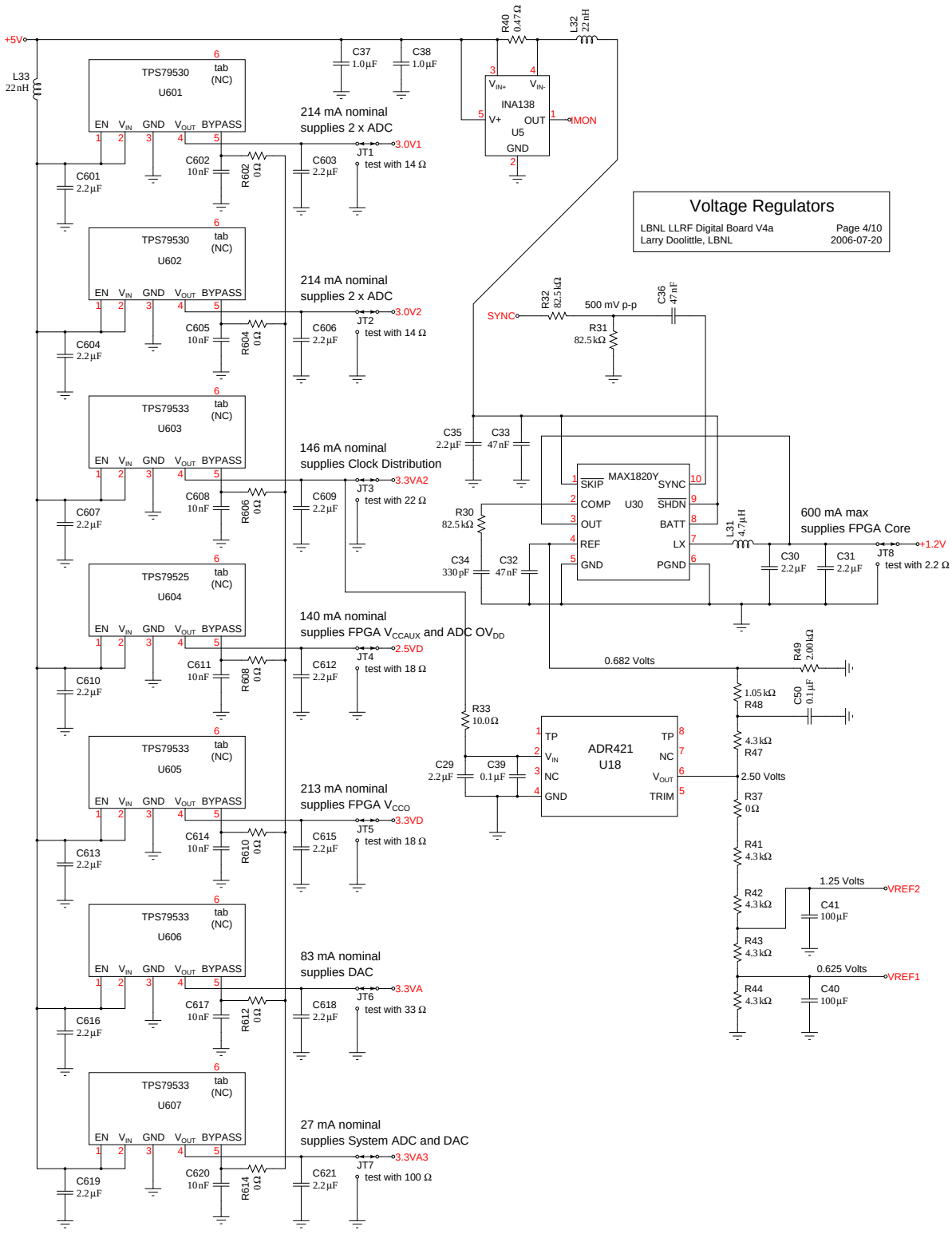
Voltage Regulators
LBNL LLRF Digital Board V4a
Larry Doolittle, LBNL
Page 4/10
2006-07-20
+5V
L33 22 nH
TPS79530 U601
TPS79530 U602
TPS79533 U603
TPS79525 U604
TPS79533 U605
TPS79533 U606
TPS79533 U607
tab (NC)
EN VIN GND VOUT BYPASS
C37 1.0 µF
C38 1.0 µF
R40 0.47 Ω
L32 22 nH
INA138 U5
VIN+ VIN- V+ OUT GND
IMON
214 mA nominal supplies 2 x ADC
3.0V1
3.0V2
JT1 test with 14 Ω
JT2 test with 14 Ω
C601 2.2 µF
C602 10 nF
R602 0 Ω
C603 2.2 µF
C604 2.2 µF
C605 10 nF
R604 0 Ω
C606 2.2 µF
SYNC
R32 82.5 kΩ
500 mV p-p
C36 47 nF
R31 82.5 kΩ
C35 2.2 µF
C33 47 nF
MAX1820Y U30
SKIP COMP OUT REF GND
SYNC SHDN BATT LX PGND
R30 82.5 kΩ
C34 330 pF
C32 47 nF
L31 4.7 µH
600 mA max supplies FPGA Core
+1.2V
C30 2.2 µF
C31 2.2 µF
JT8 test with 2.2 Ω
146 mA nominal supplies Clock Distribution
3.3VA2
JT3 test with 22 Ω
C607 2.2 µF
C608 10 nF
R606 0 Ω
C609 2.2 µF
140 mA nominal supplies FPGA VCCAUX and ADC OVDD
2.5VD
JT4 test with 18 Ω
C610 2.2 µF
C611 10 nF
R608 0 Ω
C612 2.2 µF
0.682 Volts
R49 2.00 kΩ
1.05 kΩ R48
C50 0.1 µF
R33 10.0 Ω
ADR421 U18
TP VIN NC GND
TP NC VOUT TRIM
C29 2.2 µF
C39 0.1 µF
4.3 kΩ R47
2.50 Volts
R37 0 Ω
213 mA nominal supplies FPGA VCCO
3.3VD
JT5 test with 18 Ω
C613 2.2 µF
C614 10 nF
R610 0 Ω
C615 2.2 µF
R41 4.3 kΩ
R42 4.3 kΩ
1.25 Volts
VREF2
C41 100 µF
R43 4.3 kΩ
0.625 Volts
VREF1
R44 4.3 kΩ
C40 100 µF
83 mA nominal supplies DAC
3.3VA
JT6 test with 33 Ω
C616 2.2 µF
C617 10 nF
R612 0 Ω
C618 2.2 µF
27 mA nominal supplies System ADC and DAC
3.3VA3
JT7 test with 100 Ω
C619 2.2 µF
C620 10 nF
R614 0 Ω
C621 2.2 µF

FPGA Power Capacitors

LBNL LLRF Digital Board V4a — Page 5/10
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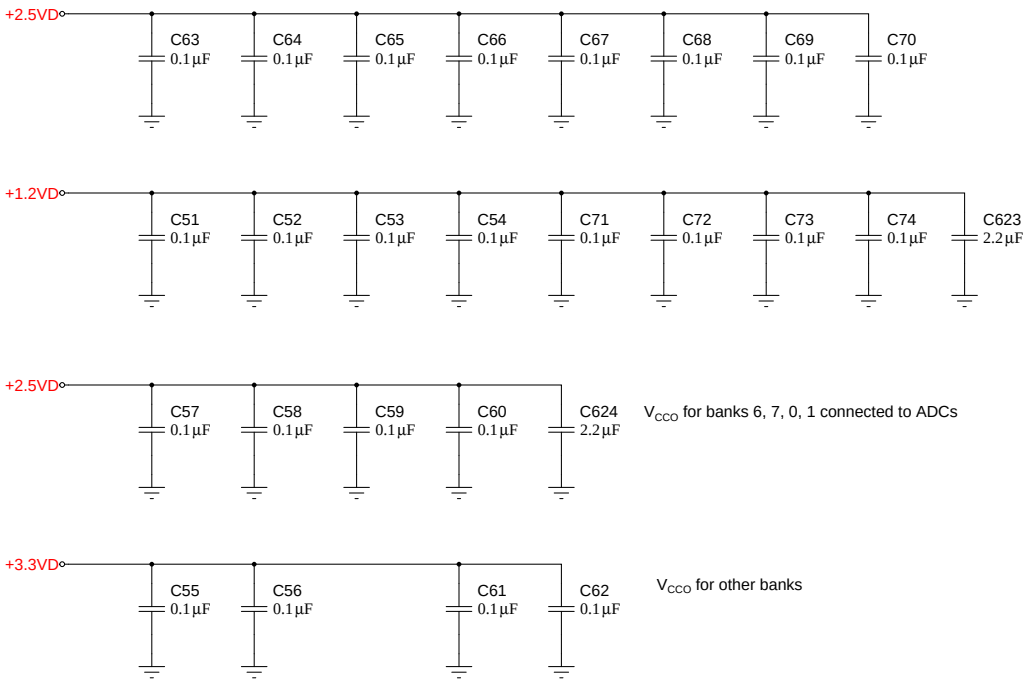

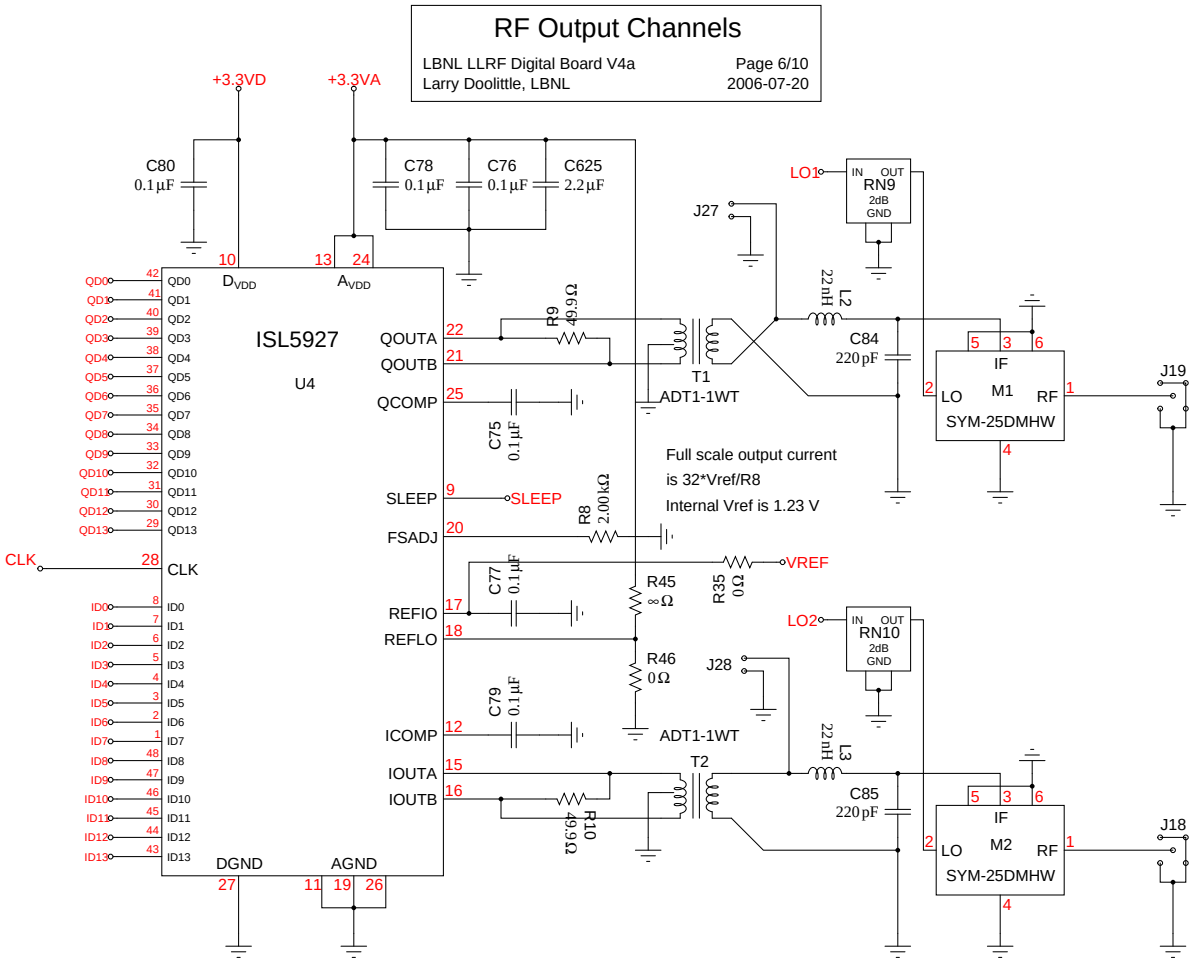
RF Output Channels
LBNL LLRF Digital Board V4a
Larry Doolittle, LBNL
Page 6/10
2006-07-20
+3.3VD
+3.3VA
C80
0.1µF
C78
0.1µF
C76
0.1µF
C625
2.2µF
ISL5927
U4
DVDD
AVDD
DGND
AGND
QD0
QD1
QD2
QD3
QD4
QD5
QD6
QD7
QD8
QD9
QD10
QD11
QD12
QD13
CLK
ID0
ID1
ID2
ID3
ID4
ID5
ID6
ID7
ID8
ID9
ID10
ID11
ID12
ID13
QOUTA
QOUTB
QCOMP
SLEEP
FSADJ
REFIO
REFLO
ICOMP
IOUTA
IOUTB
R9
49.9Ω
R8
2.00kΩ
C75
0.1µF
C77
0.1µF
C79
0.1µF
R45
∞Ω
R46
0Ω
R35
0Ω
R10
49.9Ω
T1
ADT1-1WT
T2
ADT1-1WT
VREF
J27
J28
LO1
LO2
RN9
RN10
2dB
IN
OUT
GND
L2
22nH
L3
22nH
C84
220pF
C85
220pF
IF
LO
RF
M1
M2
SYM-25DMHW
J19
J18
Full scale output current
is 32*Vref/R8
Internal Vref is 1.23 V

Clock Distribution

LBNL LLRF Digital Board V4a — Page 7/10
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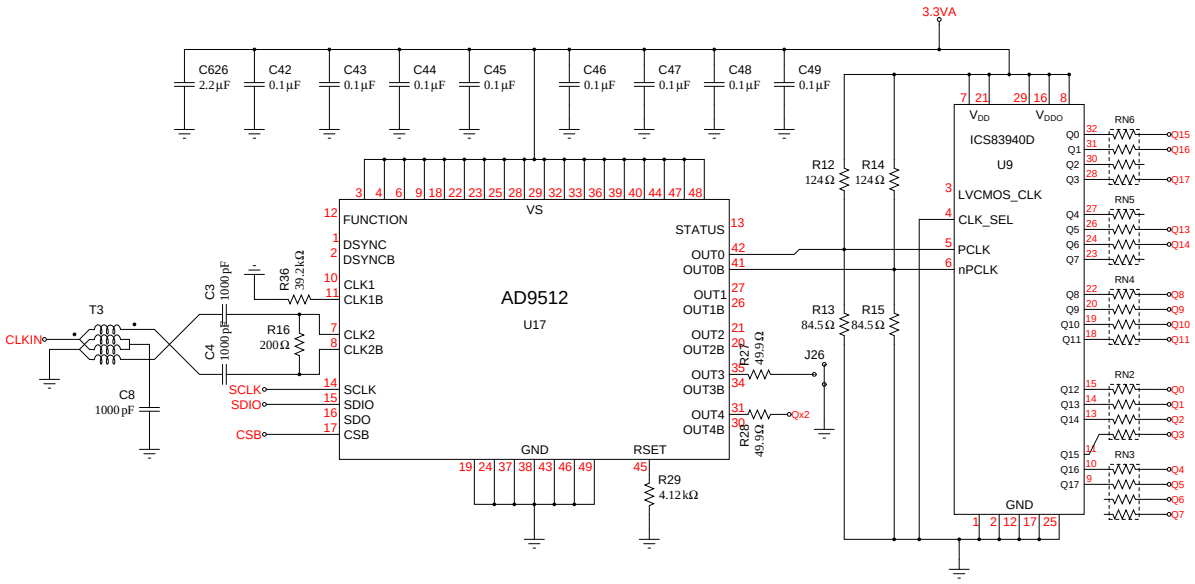

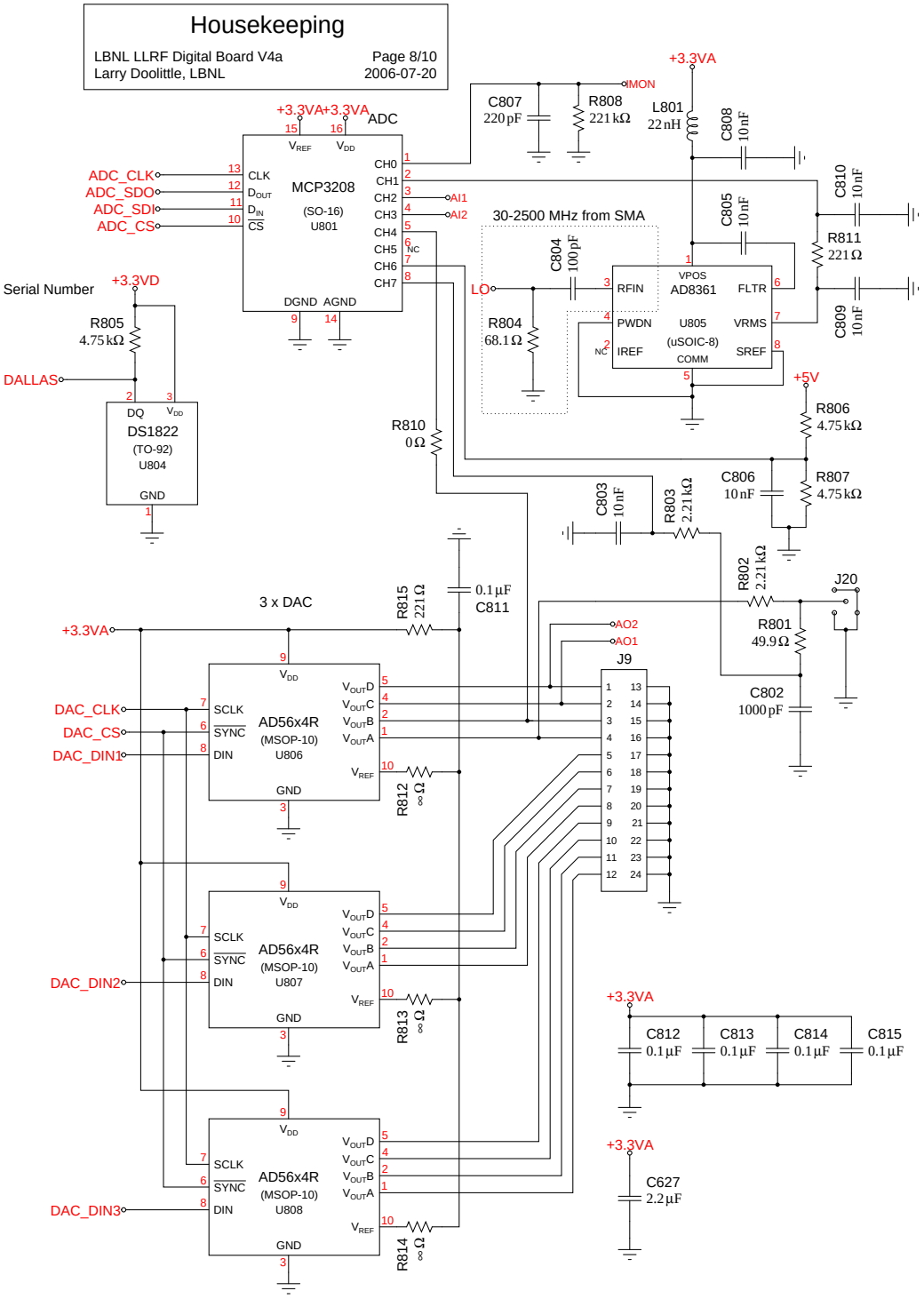
Housekeeping
LBNL LLRF Digital Board V4a
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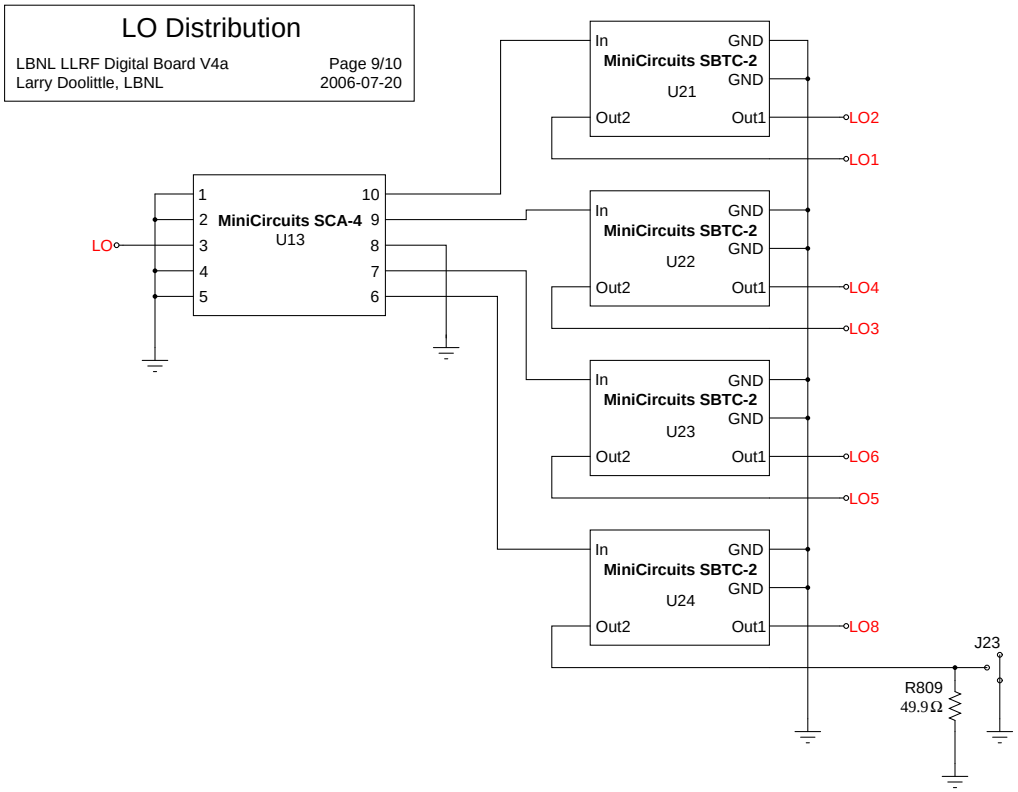
Page 8/10
2006-07-20
+3.3VA
IMON
C807
220 pF
R808
221 kΩ
L801
22 nH
C808
10 nF
+3.3VA+3.3VA
ADC
ADC_CLK
ADC_SDO
ADC_SDI
ADC_CS
MCP3208
(SO-16)
U801
AI1
AI2
30-2500 MHz from SMA
C804
100 pF
C805
10 nF
C810
10 nF
R811
221 Ω
C809
10 nF
LO
AD8361
VPOS
RFIN
FLTR
PWDN
VRMS
IREF
SREF
COMM
U805
(uSOIC-8)
R804
68.1 Ω
Serial Number
+3.3VD
R805
4.75 kΩ
DALLAS
DS1822
(TO-92)
U804
GND
+5V
R806
4.75 kΩ
R810
0 Ω
C806
10 nF
R807
4.75 kΩ
C803
10 nF
R803
2.21 kΩ
R802
2.21 kΩ
J20
R801
49.9 Ω
C802
1000 pF
3 x DAC
R815
221 Ω
0.1 µF
C811
+3.3VA
AO2
AO1
J9
DAC_CLK
DAC_CS
DAC_DIN1
DAC_DIN2
DAC_DIN3
SCLK
SYNC
DIN
AD56x4R
(MSOP-10)
U806
U807
U808
GND
R812
∞ Ω
R813
∞ Ω
R814
∞ Ω
+3.3VA
C812
0.1 µF
C813
0.1 µF
C814
0.1 µF
C815
0.1 µF
+3.3VA
C627
2.2 µF


LO Distribution
LBNL LLRF Digital Board V4a
Larry Doolittle, LBNL
Page 9/10
2006-07-20
LO
1
2
3
4
5
10
9
8
7
6
MiniCircuits SCA-4
U13
In
GND
MiniCircuits SBTC-2
GND
U21
Out2
Out1
LO2
LO1
U22
LO4
LO3
U23
LO6
LO5
U24
LO8
J23
R809
49.9Ω

Interlock Input/Output

LBNL LLRF Digital Board V4a — Page 10/10
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