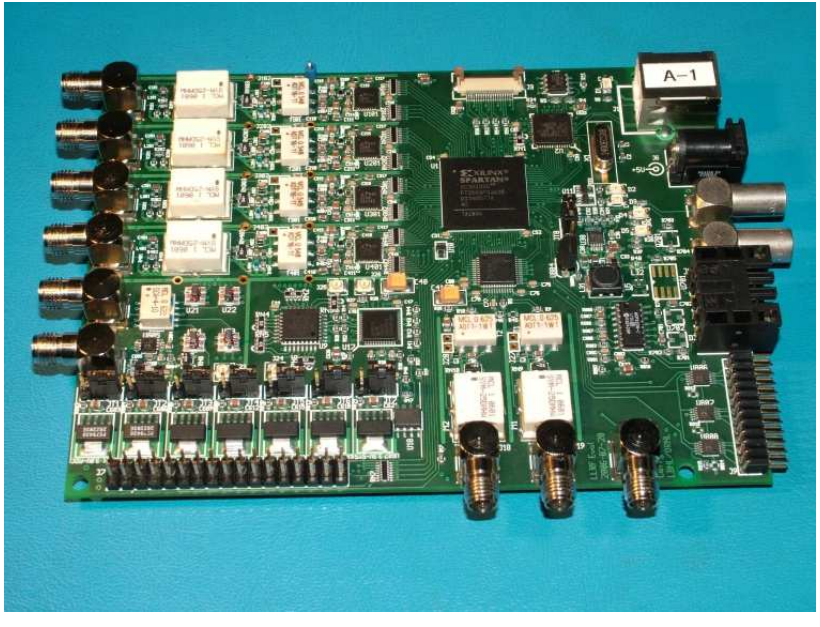
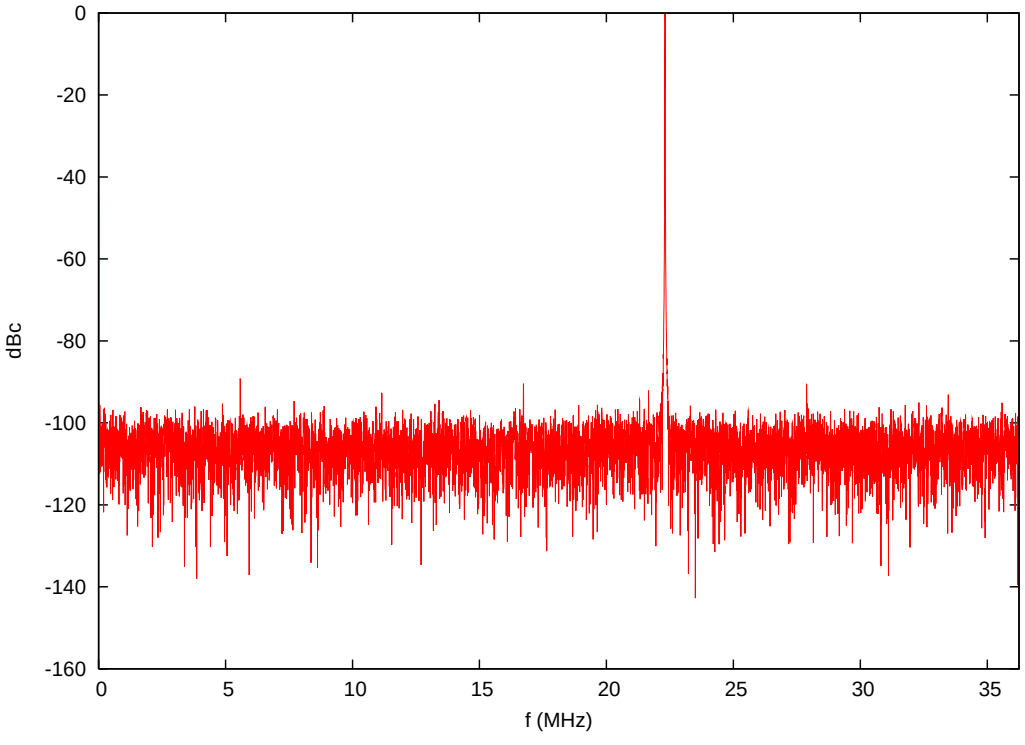
LLRF4 Board

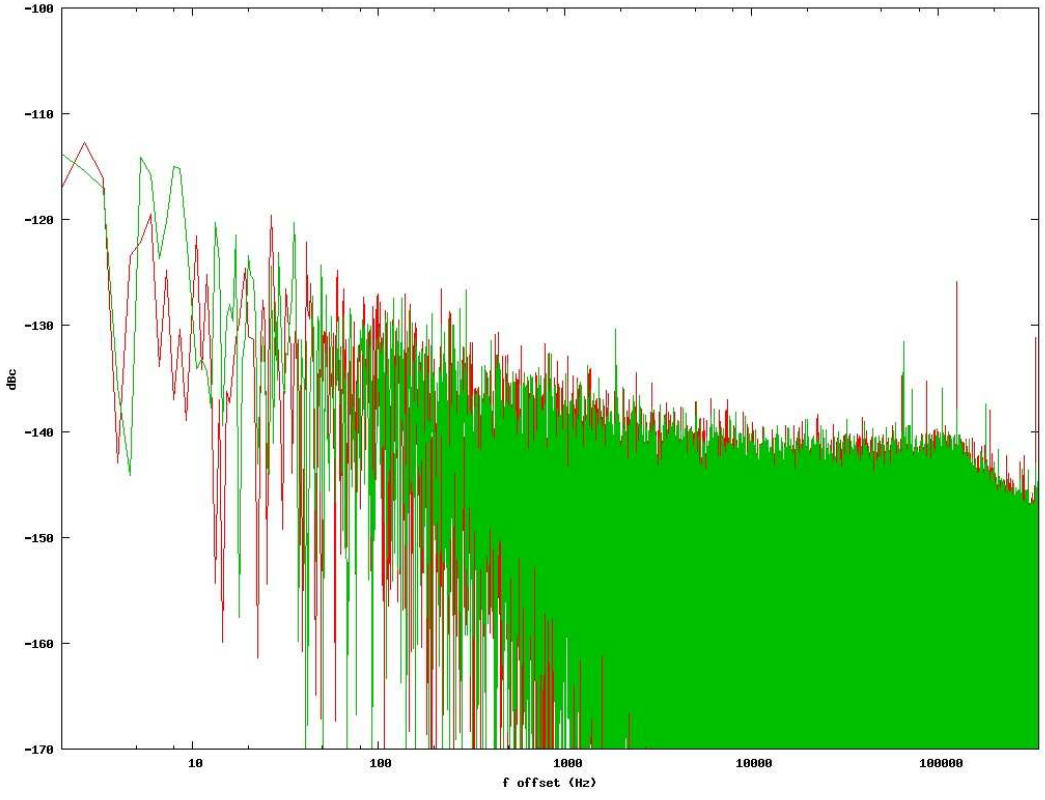
Larry Doolittle, LBNL, with support from FNAL and ORNL
Status as of May 21, 2007



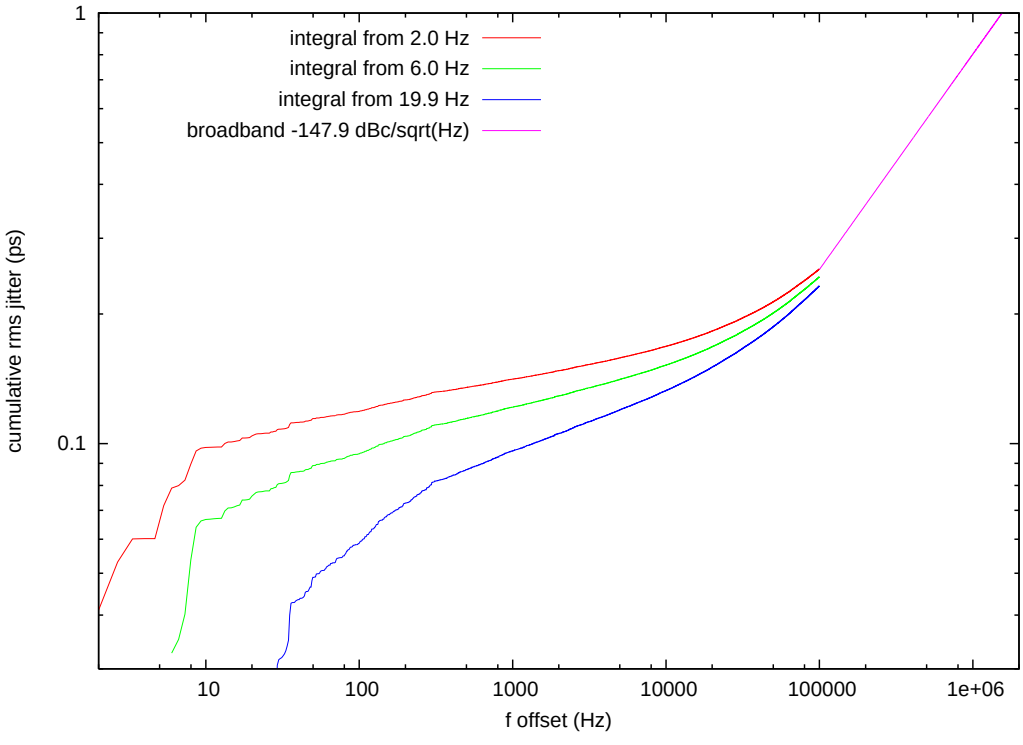
All digital and analog working (with some white wires).
RF up/down conversion bypassed because of problems with LO distribution.
1 board physically at LBNL, 1 at ANL, and 4 at ORNL.



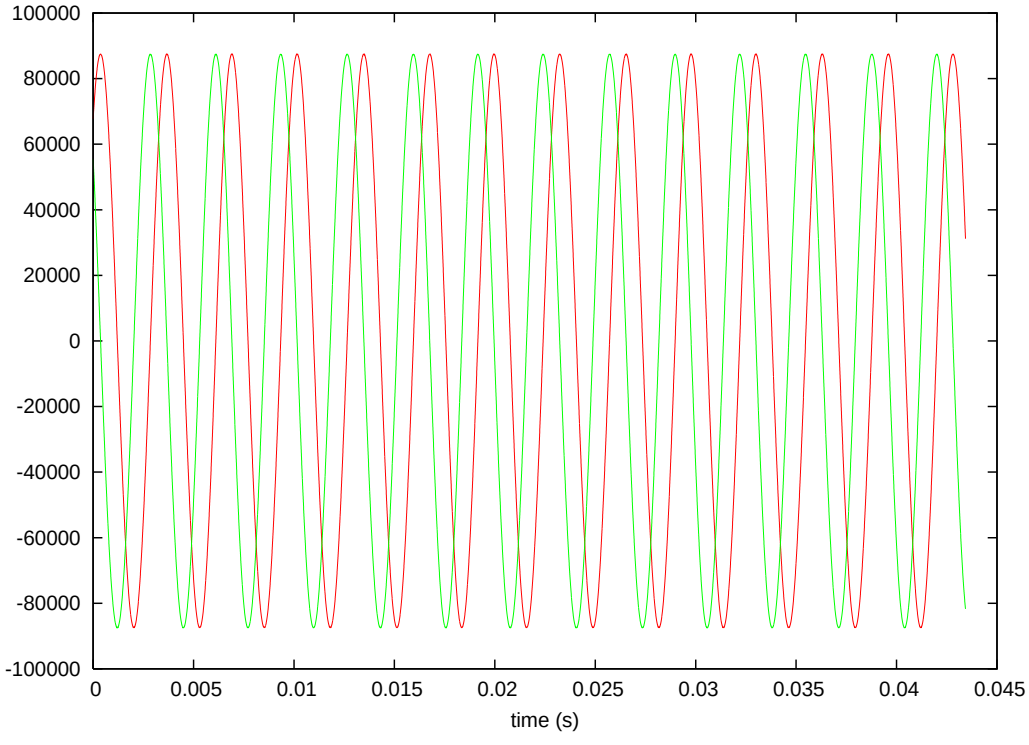
Two boards, common clock (290 MHz), DAC output of one board routed through amplifier and filters to ADC input of second board. Single tone 9/13 of ADC clock. Largest distant spur -89 dBc 3rd harmonic (5.6 MHz).



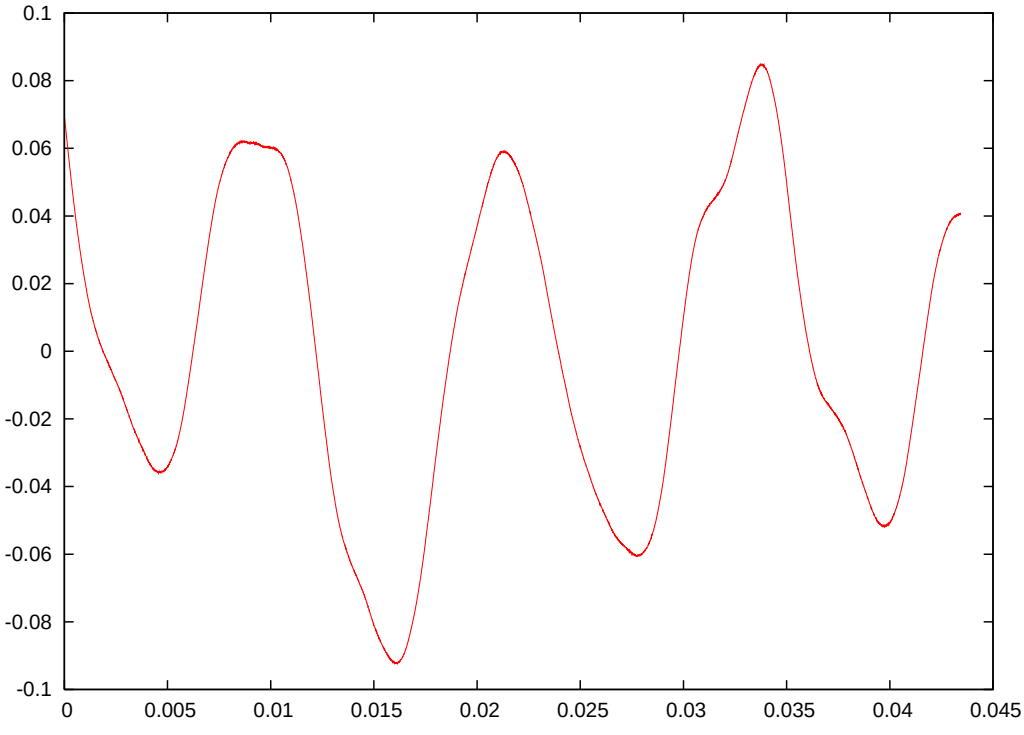
Largest close-in spur -126 dBc at 127.4 kHz offset. $1/f$ corner around 3 kHz: I can infer (but not prove) that noise comes from the ZFL-1000H external amplifier.



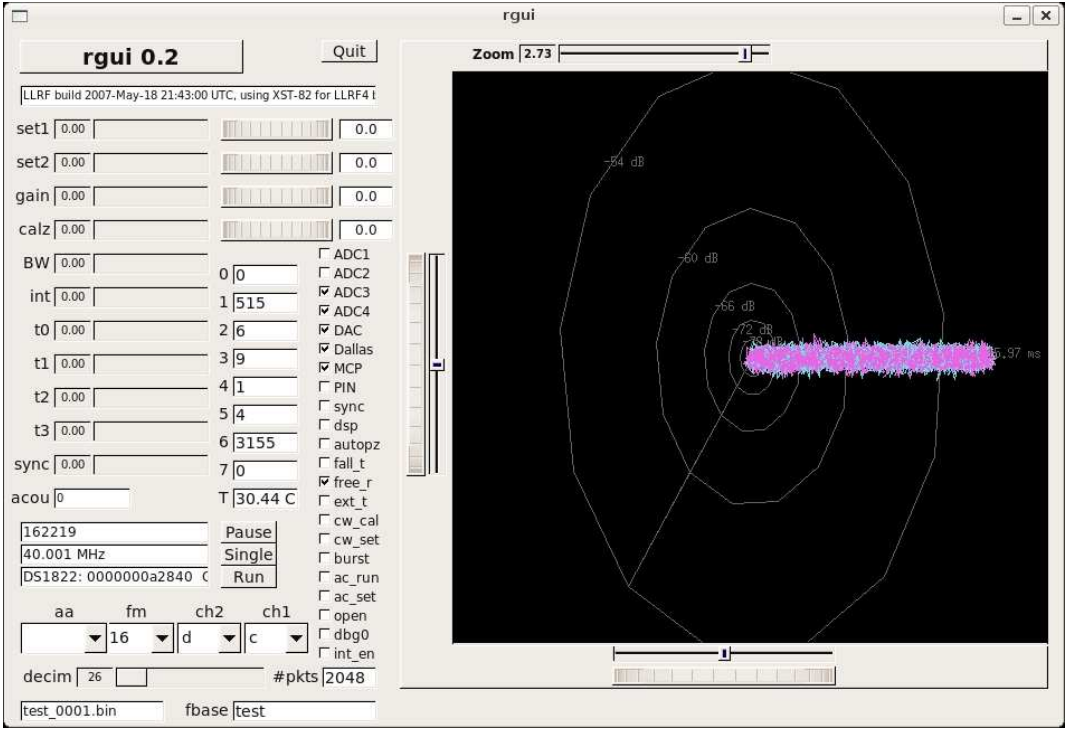
High frequency noise cutoff is normally considered the cavity closed loop bandwidth, less than 100 kHz. Low frequency cutoff based on how often the the system can digitally "autozero" to a phase reference.



Crude SEL operation on the Argonne 345 MHz triple spoke cavity.



Phase fluctuations in SEL after software subtraction of a 306.4 Hz offset.



Working hard to make FPGA and host software useful. About 6000 lines of Verilog, current builds use about 68% of FPGA.