RTDL IP Module Specifications
Draft ver. 0.2

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Introduction

The RTDL IP module functionality includes

- an IP module Interface,
- one Event Link Interface,
- one Real Time Data Link Interface (RTDL) and
- resources for implementing parts of the *V105 RTDL encoder module*, *V123 Beam Synchronous Encoder Module* and *V124 Beam Synchronous Trigger Module* functionality.

IP Specifications

The LBL RTDL IP module is compliant with the specifications of IP modules as defined in

IP Module Specification, Draft 1.0d.0, GreenSpring Computers, Inc.
http://wwwinfo.cern.ch/ce/ms/mezzanines/vita4.pdf.

The following IP functions are supported:

1. Single Size **Type III** IP module
2. 16 bit support (firmware can use 8 or 16 bit wide access)
3. 8MHz and 32MHz operation
4. ID PROM Format II support
5. full IO space (128 Bytes) support
6. full memory space (8MBytes) support
7. Byte and Word addressing
8. Two interrupts (user programmable)
9. Interrupt Acknowledge
10. IO and MEM DMA channel support (but at this point not part of the firmware design requirements)
11. +5V/1A max. power consumption

IP Specifications and Recommendation violations

1. **3.3V/5V tolerant physical signal interface**

   The IP standard was written at a time when 5V TTL and CMOS logic were still in common use, albeit it was accepted by the time the standard was released, that 5V logic was a thing of the past. Today it is virtually impossible to design a modern product around true 5V interfaces without serious degradation in product performance, reliability and without an increase of cost and part count. The most devastating consequence of regression at this time would be the use of components which are already being phased out. This would make product support very hard and expensive, if not unrealistic.

Despite the 5V CMOS with TTL threshold logic requirements of the IP standard there is no technical reason to comply with it in this particular point. The technical solution to this dilemma is the industry wide accepted choice of 5V tolerant IO signals with 3.3V driver levels. This is and will still be for a couple of years supported by programmable logic manufacturers. The only drawbacks are considerably smaller noise margins and additional non-trivial timing delays for slowly rising or falling waveforms (leading to a potential duty-cycle violation for clock signals).
If this IP card is used on a carrier board which does not adhere to good design techniques for fast signals and power/ground connections, the board and or the carrier could malfunction.

2. Mechanical Type III board request

The RTDL IP board covers the functionality of 2-3 VME boards and is a potentially dense design. This draft takes the freedom to define the board as a Type III IP board. Type III boards are not subjected to height restrictions for component assembly on the back side of the board. This allows to include high components like connectors and fiber optic receivers. If this request turns out to be unnecessary or if the board height is a crucial user requirement, the final product will be re-classified as a Type II board (max. 0.072" backside component height) and only functions fitting into the restrictions of a Type II board will be implemented.

NOTE: At this point a Type II implementation is very likely but Type III can not be ruled out, yet. A Type I implementation (no components on the backside allowed) would be too restrictive and can be ruled out.

Event Link Interface Specifications

The event link interface is in accordance of the specifications of the *V123 Beam Synchronous Encoder Module* document. The circuit implementation will be differ from the original hardware to accommodate the needed functionality in the given mechanical restrictions of the IP form factor while trying to maintain as many of the logical functions as possible.

Event Link transceiver characteristics

1. 1 Start bit , 8 Data bit, 1 Parity bit, 2 Stop bit data format.
2. Synchronous 12 bit frame bi-phase mark 1 encoding.
3. No explicit frame boundary code.
4. Idle line representation: bi-phase encoded 1's.
5. 30-70MHz PLL center frequency f_0 (set by VCO tank circuit inductor value).
6. f_0+-10% PLL lock range.
7. 10ps short time PLL jitter.
8. Link active, PLL lock detection.
9. Differential outputs, transformer coupled, 50Ohm capable line driver, +-2V signal level

for 6dB line loss compensation.
10. 50Ohm terminated, transformer coupled differential inputs.
11. Digital jitter reduction filter technology for degraded signals (on long lines).

RTDL Interface Specifications

RTDL transceiver characteristics

1. 1 Start bit , 8 parameter ID bit, 24 Data bit, 1 Parity bit, 1 Stop bit data format.
2. Synchronous 35 bit frame bi-phase mark 1 encoding.
3. No explicit frame boundary code.
4. Idle line representation: bi-phase encoded 1's.
5. 30-70MHz PLL center frequency f_0.
6. f_0+-10% PLL lock range.
7. 10ps short time PLL jitter.
8. Link active, PLL lock detection.
9. Differential outputs, transformer coupled, 50Ohm capable line driver, +-2V signal level for 6dB line loss compensation.
10. 50Ohm terminated, transformer coupled differential inputs.
11. Digital jitter reduction filter technology for degraded signals (on long lines).

Compatibility

Unfortunately the clock recovery circuit of the available V123 implementation can not be embedded into the IP board hardware without risk of serious degradation of the targeted performance. Since the IP board is specifically designed as a high quality clock source for high speed digitizer boards, the goal of (programmable logic) design compatibility to the old system can not be achieved and the RTDL implementation has to be re-written.

However, the user interface, i.e. the register map etc. will be made identical to the exisiting boards, so that, with maybe minor modifications to adapt from the VME to the IP bus, existing software will work with this board.

V105, V123 and V124 functionality

A subset of functions from the *V105*, *V123* and *V124* functionality can be implemented within the resources of the IP RTDL board. The selection of these functions can happen after prototyping since the resources of the used FPGA are not the limiting factor. Only digital IO functions with 3.3V CMOS levels can be supported.

IO-Connector Pinout

The IP board's IO connector carries the following five differential, transformer coupled signals:

- EventLink inputs
  - EL_IN+
  - EL_IN-
  - EL_IN_COM

- EventLink outputs
  - EL_OUT+
  - EL_OUT-
  - EL_OUT_COM

- Restored EventLink clock signal (EventLink BaudRate x 4, 68MHz. nom.)
  - EL_CLK+
  - EL_CLK-
  - EL_CLK_COM

- RTDL input signals
  - RTDL_IN+
  - RTDL_IN-
  - RTDL_IN_COM

and finally

- RTDL output signals
  - RTDL_OUT+
  - RTDL_OUT-
  - RTDL_OUT_COM.

The pinout chosen for these pins (Diagram 1) optimizes symmetry and improves routing on the IP PCB board.

User logic IO signals

There are 20 general purpose 3.3V logic signals called USER13-15, USER17-19, USER21-24, USER38-40, USER42-44 and USER46-49 and a total of six GND pins.

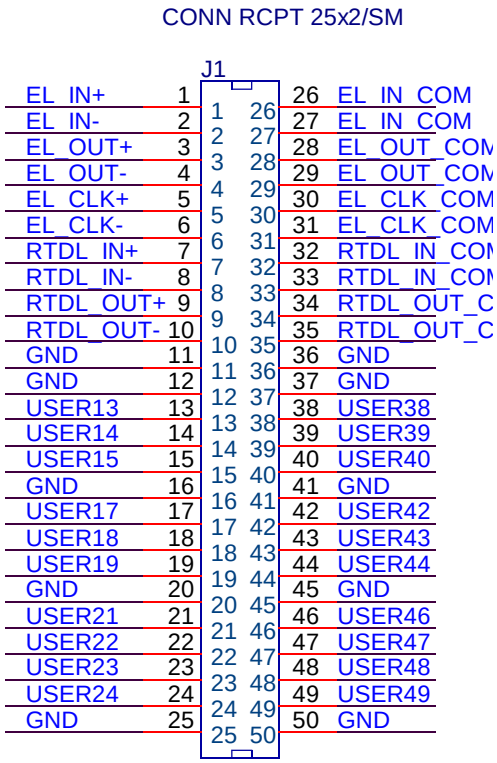

Diagram 1: IP IO pin connector pinout